**Project 4 Evaluation**

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| Name: | | Total: | |
| Checklist | Weight | Earned | Notes |
| 1. Write C/C++ code for the CORDIC circular mode module using VivadoHLS | 25 |  |  |
| 1. Write testbench code to verify the function of the C/C++ code code in VivadoHLS | 10 |  |  |
| 1. Architecture optimization, constraint configurations and advantages of final design. | 10 |  |  |
| 1. Model Composer model using the VivadoHLS block and testing results. | 10 |  |  |
| 1. Synthesis and place and route implementation report. | 5 |  |  |
| 1. Hardware in the loop Co-Simulation to verify performance of VivadoHLS code on the ZedBoard in the lab. | 5 |  |  |
| 1. Results comparison with the built-in Xilinx CORDIC modules in SysGen in terms of numerical results and also FPGA area usage. | 10 |  |  |
| 1. IP block export to SDK and Zynq ARM program control | 20 |  |  |
| 1. Turning in files | 5 |  |  |